WHAT IS CLAIMED IS:

1. A bias circuit having a start-up circuit, comprising:

a bias circuit part using a current mirror circuit, and for generating a constant bias voltage to an output node from a power source voltage as applied, and

a start-up circuit part having a capacitor connected between the output node and a common node of in common connecting gates of MOS transistors constructing the current mirror circuit.

2. The bias circuit as claimed in claim 1, wherein the bias circuit part includes:

a first PMOS transistor having a source thereof connected to the power source voltage;

a second PMOS transistor having a gate and a drain thereof connected to a gate of the first PMOS transistor to form the common node, and having a source thereof connected to the power source voltage;

a first NMOS transistor having a drain and a gate thereof connected to a drain of the first PMOS transistor to form the output node, and having a source thereof connected to a grounded power source;

a second NMOS transistor having a drain thereof connected to the drain of the second PMOS transistor, and having a gate thereof connected to the gate of the first NMOS transistor; and

a resistor connected between the source of the second NMOS transistor and the grounded power source.

3. A bias circuit having a start-up circuit, comprising:

a bias circuit part using a cascode current mirror circuit of a double-stage current mirror circuit, and for generating a constant bias voltage to an output node from an applied power source voltage; and

a start-up circuit part for actuating the bias circuit part upon an initial application of the power source voltage, the start-up circuit part including:

a first capacitor connected between a first common node connecting in common gates of first MOS transistors constructing a first single-stage current mirror circuit of the cascode current mirror circuit and a second common node connecting in common gates of second MOS transistors constructing a second single-stage current mirror circuit; and

a second capacitor connected between the second common node and the output node.